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Article

A Simple Multilevel Space Vector Modulation Technique and MATLAB System Generator Built FPGA Implementation for Three-Level Neutral-Point Clamped Inverter

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Abstract: The pulse width modulation (PWM) is an important segment in power electronic inverters and multilevel inverters (MLIs) design. The space vector modulation (SVM) methods own distinct advantages over other PWM methods. However, MLI SVM has involved more mathematics in their executions. Hence, the digital signal processors (DSPs) or field programmable gate arrays (FPGAs) based digital implementations are highly preferred for MLI SVM realizations, which require exceptional properties. The conventional MLI SVMs use complex mathematical functions to solve their internal functions to identify the space vector diagram (SVD) sub-triangle and over modulation boundary switching on-times. Particularly these are the changes in the position of reference vector with respect to their sub-triangle positions involving higher mathematical functions. This paper proposes a simplified three-level MLI SVM that reduces the sub-triangle and over modulation switching on-time calculations with reduced mathematical functions. The proposed MLI SVM is derived based on two-level SVM without changing the reference vector position, unlike the traditional approaches. This helps in extending the SVM for any n-level inverter with additional LUTs. The detailed theoretical study, MATLAB-Simulink system generator simulations and Xilinx FPGA family SPARTAN-III-3A based experimental implementations are done with three-level neutral point MLI fed induction motor drive. The theoretical design, analysis, and experimentation results validate the advantages of the proposed PWM design and its implementation. In addition, the proposed implementation is executed from the MATLAB Xilinx system generator directly into target FPGA, which makes it faithful, efficient and minimizes the time spent.

Keywords: pulse width modulation (PWM); multilevel inverter (MLI); space vector modulation (SVM); field programmable gate array (FPGA)

1. Introduction

The involvement of modern power electronics converters in the emerging technology is essential for the electrical system in the current era. Very particularly, in the overall power electronics segment, the voltage source two-level inverters are very popular and demanding, due to their application encroachment in industrial, commercial and non-conventional energy conversion systems [1]. Compared with two-level inverters, multilevel inverters (MLIs) have substantial rewards, which are intensive in the enhancement of the voltage and current waveform quality, reduction of harmonic contents, and increment of power handling capability. Nabae et al. invented the first MLI based on two-level inverter structure called neutral-point clamped (NPC) topology in 1981 [2] which was followed by the development of cascaded H-bridge (CHB), flying capacitor (FC), and hybrid MLIs in later years. Even though these MLIs are capable of producing the multi-stepped output voltages with reduced dv/dt and harmonics for improved power qualities. But, considering the DC-link capacitors balancing and common mode voltage (CMV) reduction, the MLIs are widely still investigated with different modulation strategies [3] for compensation methods. Among them, space vector modulation (SVM) offers better-quality voltage and current output with higher DC-link utilization. In addition, SVM provides a switching state selection opportunity to improve the performance of the MLI [4–15]. Particularly, the SVM contributions in NPC-MLI are widely researched and applied in the various fields of drives and renewable energy integration applications [5]. The switching selections in the multilevel SVM are mainly associated with the space vector diagram (SVD) synthesization and switching states on-time calculation. The multilevel SVM using two-level concepts are widely explored than the other MLI SVM methods [4,9,12–16]. However, these methods include complex mathematics to calculate the target reference voltage vector and recognize inner sub-triangle etc. The Zhang et al. has introduced a method for finding switching states on-time using direct two-level SVM approach. In this method, the three-level SVD has fragmented to a six, equal, two-level SVD, and its location of the centre of six virtual hexagons originated through segregation of the SVD [17]. Similar to this method, in the literature, many papers have been reported in which shifting the origin to one of the six centres, and $\alpha\beta$ -axes are rotated by 60° to use two-level on-time calculations [12–16,18–21]. Even though these methods are calculating the individual switch on-times from segregated two-level SVM, while extending to higher levels that need complex mathematical functions to calculate the sub-triangle. Seo et al. [18] proposed a scheme for an MLI SVM for three-level NPC similar to Zhang et al. where the origin is shifted to 60° which sorts six sub-hexagons to compute on-times, thereby involving additional computations. The three-level SVD based two-level SVD with reduced math function is proposed and implemented for NPC-MLI [9]. The similar idea is extended to linear modulation (LM) and over modulation (OVM) region with field programmable gate array (FPGA) implementation for NPC-MLI [19–23].

In [19], the multilevel SVD is divided into six equal two-level SVDs and switching vector on-time calculations are made through direct transformations from three neighboring switching vectors. However, the estimation of the on-time calculation is done by extending a set of matrix transformations, which includes complex computations. Extending the inverter modulation index more than 0.907 is called as OVM. It requires non-linear mathematical functions to synthesis their reference vector outside SVD hexagon [24–26]. The industrial drives, such as direct torque and field-oriented controller need OVM region operations, since linear modulation range operation restricts the inverter modulation index, and hence, the drives produce limited constant torque as it utilizes only 90% of input DC-link voltage. Hence, the inverter drive covering OVM is beneficial by means of entire exploitation of the installed input source capacity, which results in the increased cumulative speed-torque characteristics, as well as the operating boundary of the traction drives. However, OVM leads to complexities in hardware implementations, due to non-linearity switching equations [20]. Due to this complexity in the OVM region synthesization and on-time calculations, many studies are not preferred to include OVM region operation. Very few implementations have performed in the OVM region operation [21–31]. These implementations are using complex mathematical functions to realize the OVM non-linear region and on-time calculations. To realize the OVM region, the non-linear trigonometric functions are used

to find the modified on-times. These methods are relatively complex to implement [24,25]. Most of the OVM region studies in MLI SVM have been done by changing the reference vector position [23,24,26–30]. The on-time switching calculations of OVM using virtual vectors were recognized by using modifying hexagonal trajectory. However, in these methods, there would be portions of the line cycle, where the preferred reference vector could not be synthesized [28], [30]. Few algorithms were developed which use additional switching time derived from the outside hexagonal boundary projection [26,29]. However, these methods are introducing lower frequency harmonics, which are affecting the output waveform quality.

The rapid developments in high-performance microcontrollers, DSPs and FPGAs, have encouraged the research of work on digital PWM for rapid prototyping. Due to the development of ASIC technology, the FPGA based implementations have become popular, since it has an ability to implement custom hardware solutions and reprogramming flexibility. The SVM implementations on FPGA are showing a higher interest in the current era [6,12,14,32–44]. These implementations are mainly done through Altera and Xilinx Spartan family. The first successful single chip FPGA implementation of SVM has been presented by Tzou et al. [33], and followed by a variety of single chip FPGA IP core three-level SVM implementation and reported the validation [34–36,40]. These implementations have been done through Altera Vertex and Spartan with large device utilization and computational time. These direct VHDL code based implementations have suffered from the drawbacks of computational burden (writing VHDL/Verilog coding), high device utilization, and higher time taken. Particularly at high modulation ranges, due to the higher mathematical burden, the processing time is being increased [23,29,42]. These methods are very effective for implementation in terms of calculating the switching vectors and dwell times by means of simple addition and comparison operators without using any angles, trigonometric function and LUTs. However, the extension to OVM in n-level needed high mathematical operations and high hardware resources. The low complexity and fewer computation approaches make the SVM implementations very suitable for real-time application drive systems. The FPGA Spartan processors are developed on a VHDL code to carry out the implementation into FPGA. By the use of Xilinx system generator ISE tools, the SVM implementations have focused on increasing the processing speed, reduce the device utilization and the reconfiguration (partial and full) implementations [37,40]. In any implementation, the resource (FFs, LUTs) utilization is a major factor. Wang et al. [45] deployed three-level SVM in Spartan-3 FPGA with the consumption of 3,584 slices. Few more attempts were made with the same FPGA, which were also found to have higher resource utilization [14,23,40]. As an alternative, the same can be achieved using MATLAB/Simulink-Xilinx System generator tools with foundation ISE tools [46].

From the wide range of literature in the MLI SVM design and FPGA implementations, the existing methods involve higher computational complications for finding reference vector location and the on-time calculations of switching states. Hence, the existing FPGA implementations occupy higher device utilization and processing time. The reference vector positions in the multilevel SVD sub-triangle and over modulation boundary on-time calculations need to be rethought. Subsequently, the FPGA digital implementations era facilitates the exploitation of control degree of freedom in both LM and OVM region. Therefore, in this paper, a reduced mathematical approach is developed for identifying the sub-triangles and over modulation boundary area for calculating switching on-times. The proposed SVM has a direct way for calculating the LM and OVM switching times using two-level SVM. The proposed SVM is simulated using MATLAB-Simulink ISE system generator and validated directly in Xilinx family SPARTAN-III-3A XC3SD1800A-FG676 DSP-FPGA processor board. The implementation is verified through a three-level NPC-MLI fed induction motor drive laboratory prototype, and the test is performed over a wide range of operating conditions. The proposed SVM and their FPGA implementations are compared with the other reported methods. The theoretical design, analysis, and experimentation results validate the advantages of the proposed PWM design and its implementation.

The organization of the paper is deliberate as follows: Section 2 explains the space vector PWM theory for two-level and multilevel. Section 3 deals with the proposed simplified MLI SVM, including both linear and over modulations. Section 4 accomplishes the MATLAB-Simulink implementation, and Section 5 discusses the FPGA collaborated experimentation setup of three-level MLI. Sections 6 and 7 deal with the distributed implementation of MLI SVM in FPGA MATLAB XSG-ISE and experimental results. In conclusion, the rewards of the proposed MLI SVM and its implementation are presented in Section 8. The list of abbreviations and references are given in the end.

2. State of Art of Space Vector PWM Theory for Two-Level and Multilevel

2.1. Two-Level Space Vector Modulation

Figure 1a shows the SVD of a two-level inverter [37]. Here, every sector (represented as S_i , where $i = 1$ to 6) is an equilateral symmetrical triangle with the height of $h (= \sqrt{3}/2)$. Here the edge vectors (V_1 to V_6) are named as non-zero (active vectors) and V_0 and V_7 are called zero vectors. The on-time calculation of SVM switching in any sector is calculated among three nearest switching vectors (one zero vector and two active vectors). The movement of the reference or target vector V^* positioning inside the sector is synthesizing the switching times. To understand the two-level switching of SVD, the sector-1 is considered here, as shown in Figure 1b. The volts-second of V^* is determined by multiplication of V^* and sampling time (T_s). Then the time integral of V^* is estimated through the summation of products of the two of non-zero vectors (V_1 and V_2 by referring sector-1) and their time widths (T_1 and T_2).

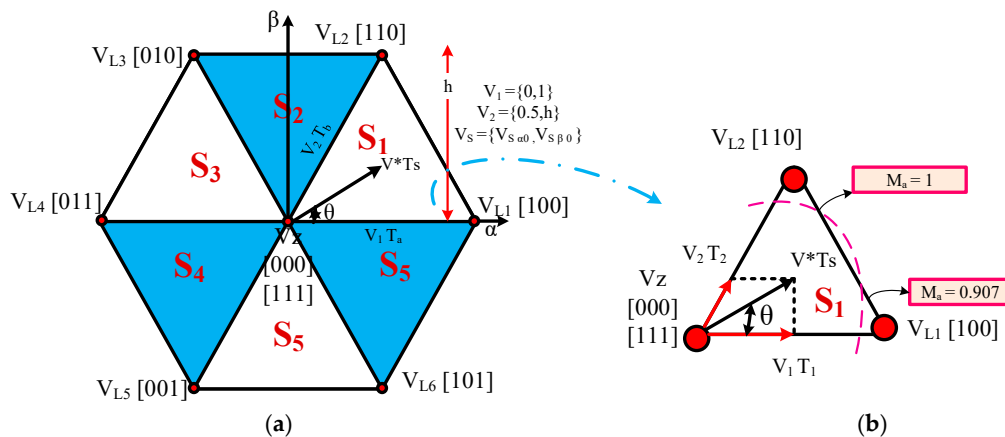


Figure 1. (a) Space vector diagram (SVD) for two-level inverter, (b) sector-1 for two-level inverter SVD.

The reference voltage V^* volts-sec equation for the sector-1 is calculated as,

$$V^*T_s = T_1V_1 + T_2V_2 + T_0V_0 \quad (1)$$

where T_1 and T_2 represents time(sec) widths of adjacent switching vectors V_1 and V_2 correspondingly, and T_0 represents as time (sec) width of zero vector (V_0). This zero vector state can be either $[000]$ or $[111]$ switching state, or else both. The movement of V^* angle (θ) within the sector is computed by

$$\theta = \tan^{-1}\left(\frac{V_\alpha}{V_\beta}\right). \quad (2)$$

The θ values sample the V^* in different sector (for example, when θ is 115° , the V^* approach sector-2, since sector-2 lies in an angle between 61° to 120°).

According to the V^* position, whether inside or outside the hexagonal SVD (see Figure 1), SVD is divided into linear modulation (where $M_a \leq 0.907$) and over modulation (where $M_a > 0.907$), respectively.

The total period is $T_s = T_1 + T_2 + T_0$. T_1 and T_2 are calculated from projecting V^* position along α -axis and β -axis with respect to SVD origin (zero point). Henceforth, the volts-sec equations for α -axis and β -axis are $V_{\alpha 0}^s T_s = T_1 + 0.5T_2$ and $V_{\beta 0}^s T_s = hT_2$. Thus, the active vector time can be written as, $T_2 = T_s V_{\beta 0}^s / h$ and $T_1 = T_s (V_{\alpha 0}^s - V_{\beta 0}^s) / 2h$. From the given switching frequency, the T_1 and T_2 help to find the zero voltage time T_0 .

2.2. Multilevel Space Vector Modulation

Realizing SVM for more than two-level inverter (conventional six-switch inverter) is called MLI SVM. Numerous MLI SVM are developed and employed in MLIs for different applications [4,6,12,20]. The difficulty in the multilevel SVM is its complex mathematical needs to locate the V^* and find the individual vectors. The interesting techniques are proposed in the literature to reduce the complexity of implementing the MLI SVM with reasonable inverter performances.

Any of the three-phase n -level SVD can be separated into six sectors (S_i), where $i = 1$ to 6. These sectors are further separated into $(n-1)^2$ sub-triangles (Δ_{ij}) where $j = 0$ to 3 and $i = 1$ to 6. Hence, the n -level SVD consists of n^3 switching states. For example, considering the three-level MLI SVD, as shown in Figure 2, it has 27-switching states ($3^3 = 27$) and 24-sub-triangles (No. of sub-triangles in each sector is $(3-1)^2 = 4$; therefore, $4 \times 6 = 24$) [6,9]. The switching vector for any level MLI is categorized into zero vector (ZV), short vector (SV) large vector (LV), and medium vector (MV). Here the ZV, MV and LV lie in the origin and boundary of the SVD, whereas, SV is multiple in numbers and placed in the middle portion of the SVD. Table 1 displays the three-level inverter SVD switching states.

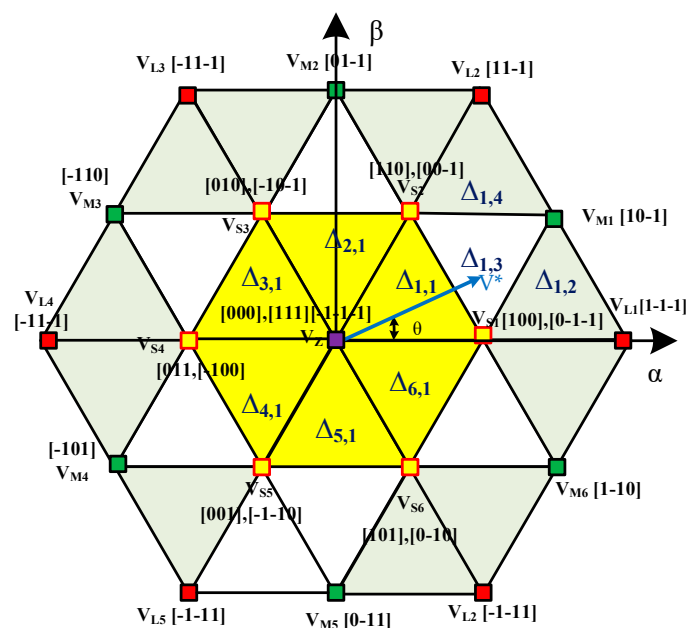


Figure 2. Three-level multilevel inverter (MLI) SVD.

Table 1. Three-level inverter SVD switching states.

| Switching vector name | Switching states | Total number of states |
|-----------------------|--|------------------------|
| ZV | [000], [111], and $[-1-1-1]$ | 3 |
| MV | [10-1], [01-1], $[-110]$, $[-101]$, [0-11], [1-10] | 6 |
| SV | [100], [0-1-1], [110], [00-1], [010], [101], [011], [100], [001], [110], [101], [0-10] | 12 |
| LV | [1-1-1], [11-1], $[-11-1]$, $[-111]$, $[-1-11]$, [1-11] | 6 |

In three-level SVD, the SVs and ZVs have redundancy-switching states that are two for SVs and three for ZVs. When the MLI level is increased, the number of redundancy-switching states for ZVs and SVs are increased.

The switching states and their on-time calculations are calculated based on the rotating reference vector, V^* position in any one of the four sub-triangles in the particular sector. For example, when V^* lies in the fourth sub-triangle of first sector ($\Delta_{1,4}$), then the nearest three vectors V_{S2} , V_{M1} and V_{L2} , switching state are used to synthesize the V^* . The duty cycle of the above nearest switching vectors δ_{VS2} , δ_{VM2} and δ_{VL2} can be calculated and applied to the pulse generations.

Fixing the V^* in the sub-triangle is the most difficult task in the SVD realizations. Few mathematical approaches have been developed for finding V^* at sub-triangle, which needed high-end digital controllers to implement them [4,7,8,16]. In addition, considering the over modulation operation in MLI, the complexity is further increased to project the trajectory location in SVD. Once the vector moves outside the hexagonal boundary of the SVD, positioning the vector in the non-linear region (unstructured boundary) is predicted from the available switching vector and its on-times. The MLI SVD over modulation implementations differ from two-level SVD [19,29,30]. In MLI SVD over modulation, the OVM boundary is operating through the crux of MVs and LVs, whereas, in two-level SVD OVM the LVs only play to synthesis the on-time calculation of OVM pulses.

3. Proposed Simplified MLI SVM for Entire Modulation Index

One of the important contributions of this paper is to propose the simple mathematical approach to find out the V^* sub-triangle position of MLI SVM. The proposed MLI SVM is developed based on standard two-level SVM for three-level MLI, and it can be extended for n-level using simple additional equations. In addition to proposed sub-triangle calculation, the reduced mathematical functions for calculating OVM switching on-times is achieved by just adding the compensated on-time gain in over modulation region with LM on-time. Hence, the proposed SVM reduces the implementation burden, since the complex part of MLI SVM calculations of sub-triangle position and OVM on-times are minimized.

3.1. Procedure in Generating MLI SVM in Linear Modulation

Figure 3 shows the three-level MLI SVM generation flowchart. Like two-level SVM, the MLI SVM takes the three-phase signal to calculate two-phase voltage vectors stationary reference frame (V_α, V_β) [20]. Then, the V_α, V_β are converted into reference voltage vector in polar form as $V^* \angle \theta$, where ' V^* ' is the voltage magnitude, and ' θ ' is the angle of the V^* .

Using V^* and θ , the reference vector sector position is calculated. Here, based on the V^* magnitude the SVD operation regions (either LM or OVM) are calculated. In Figure 3, the flow chart is handling only LM MLI SVM, where the proposed sub-triangle calculations are the same for LM and OVM.

The V^* sub-triangle location calculation with-in the sector is calculated through orthogonal time slope mathematical function in V_α, V_β plane. The stationary plane of $V_{\alpha o}^s$ and $V_{\beta o}^s$ are calculated for every T_s and then mapping for the reference vector V^* located in sub-triangle is done by comparing $V_{\alpha i}^s$ and $V_{\beta i}^s$. These logical expressions can be applied for any level for identifying the V^* sub-triangle. The next section explains the proposed sub-triangle calculations.

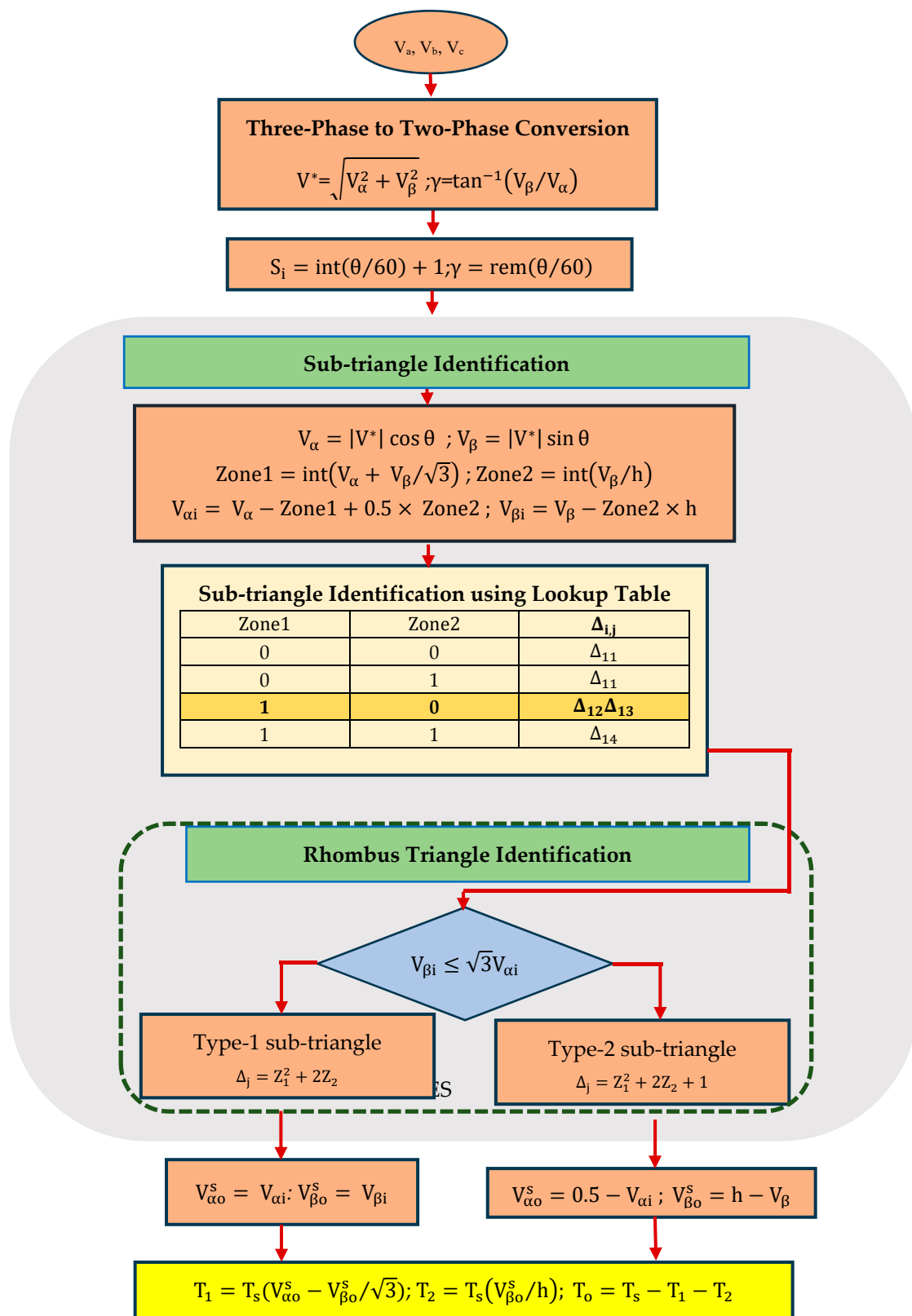


Figure 3. Flow chart for MLI SVM in LM.

3.2. Proposed Sub-Triangle Calculations

Considering the three-level multilevel SVD, shown in Figure 4, the sub-triangle 1 and 4 (type-1 triangles) can be directly calculated from the V^* magnitude, sector number and its respective sector angle (γ),

$$\gamma = \text{rem}(\theta/60). \quad (3)$$

However, this calculation does not support to calculate sub-triangle 2 and 3 (type-2 triangles). Hence, in order to handle type-1 and type-2 triangles searching progress, a simple look-up table and a searching process is developed directly from $V_{\alpha i}^s$ and $V_{\beta i}^s$. Once the V^* sub-triangle is identified, that particular sub-triangle can be considered as a sector and then two-level SVM is applied to calculate the respective sub-triangle switching states on-time calculation. The same procedure is applied to all sectors in the particular M_a and f_s . The proposed sub-triangle calculation is explained through sector-1 ($\Delta_{1,j}$) as illustrated in Figure 4.

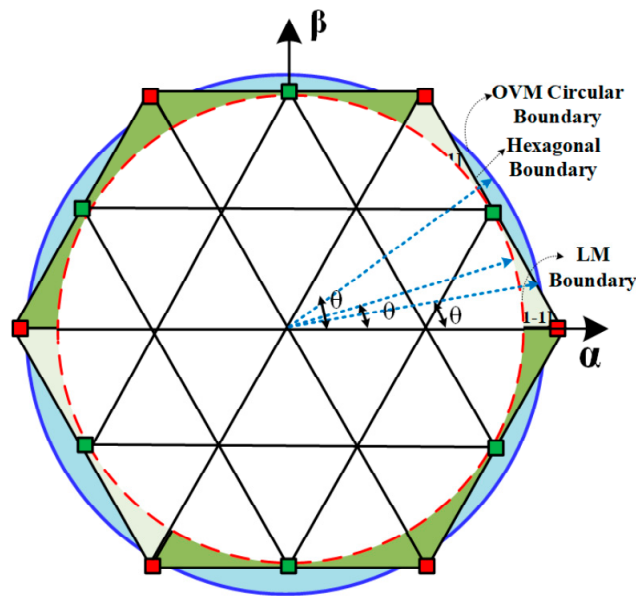


Figure 4. SVD linear modulation (LM) and over modulation (OVM) boundary.

The calculation of proposed sub-triangle involves two approaches: (1) Type-1 sub-triangles, (2) Type-2 sub-triangles. The V^* position for Type-1 triangles $\Delta_{1,1}$ and $\Delta_{1,4}$ can be calculated directly from $V_{\alpha i}^s$ and $V_{\beta i}^s$. However, the calculation of Type-2 triangles $\Delta_{1,3}$ and $\Delta_{1,2}$ (orange colored area in Figure 5b) portions are challenging. Figure 5 shows the V^* location identification for Type-1 and Type-2 triangles. According to that, the search process of the triangle of V^* can be narrowed down using the two zones in SVD (Zone-1 and Zone-2). The coordinates ($V_{\alpha 0}$, $V_{\beta 0}$) of these triangles are calculated using two integer calculations of Zone-1 and Zone-2 as follows,

$$\text{Zone1} = \text{int}(V_{\alpha} + (V_{\alpha} / \sqrt{3})), \quad (4)$$

$$\text{Zone2} = \text{int}(V_{\alpha} + h). \quad (5)$$

In Equation (4), Zone-1 integer denotes the portion of the sector among the two lines joining the vertices divided by distance 'h' and inclined at 120° with respect to α -axis. In Figure 5b, Zone-1 is valued as zero, it indicates that the point V^* is below the line B and C. The Zone-1 appears that the point V^* lies between the points A and B and D and F. The Zone-2 denotes the part of the sector between the two lines joining the vertices separated by distance 'h' and parallel to α -axis. When the Zone-2 is valued as zero, it indicates that the reference vector tip V^* is positioned between the lines A and D and C and E. When the Zone-2 is valued as integer one, it indicates that the point V^* lies above

the line C and D. Geometrically, the Zone-1 and Zone-2 values are acquired at an intersection of two rectangular regions (rhombus). Here, the V^* may be positioned either in triangle $\Delta_{1,2}$ or $\Delta_{1,3}$.

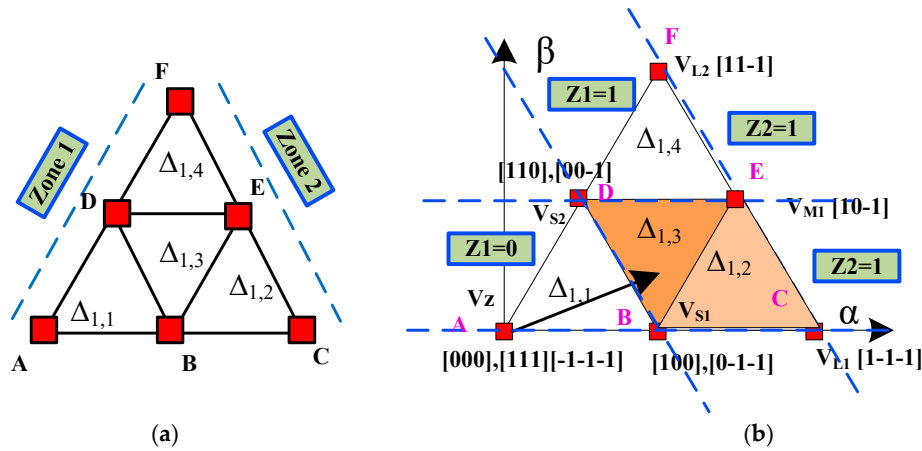


Figure 5. (a). Sector-1 with Zone, (b) sector-1 with Zone, and Type-1, Type-2 triangles.

Hence, the V^* position in type -1 triangles ($\Delta_{1,1}$ and $\Delta_{1,4}$) is directly identified from Zone-1 and Zone-2 integer values. The Zone-1 and Zone-2 receipts zero integer, when the V^* is located in a triangle $\Delta_{1,1}$. The Zone-1 and Zone-2 receipts integer one when the V^* is located in triangle $\Delta_{1,4}$. However, the other options from the Zone-1 and Zone-2 (integers of Zone-1 is zero and Zone-2 is one or Zone-1 is one and Zone-2 is zero) are not assisting in identifying the $\Delta_{1,2}$ and $\Delta_{1,3}$.

Hence, the Type-2 sub-triangles ($\Delta_{1,2}$ and $\Delta_{1,3}$) are calculated in rhombus using diagonal slope coordinate comparisons. The V^* co-ordinates point with respect to rhombus point B can be written as,

$$V_{\alpha i} = V_{\alpha} - \text{int}(\text{Zone1}) + 0.5 \text{ int}(\text{Zone2}) \quad (6)$$

$$V_{\beta i} = V_{\beta} + 0.5h \quad (7)$$

Figure 6a shows the sub-triangle $\Delta_{1,2}$ and $\Delta_{1,3}$ rhombus and its slope calculations. The sub-triangle, anywhere in reference vector V^* is situated by relating the slope of B and slope of BE. The slope B and BE can be written as,

$$V_{\beta i} \leq \sqrt{3}V_{\alpha i} \quad (8)$$

Now, comparing the Equation (8) inequality of the Type-2 sub-triangles ($\Delta_{1,2}$ and $\Delta_{1,3}$) is identified.

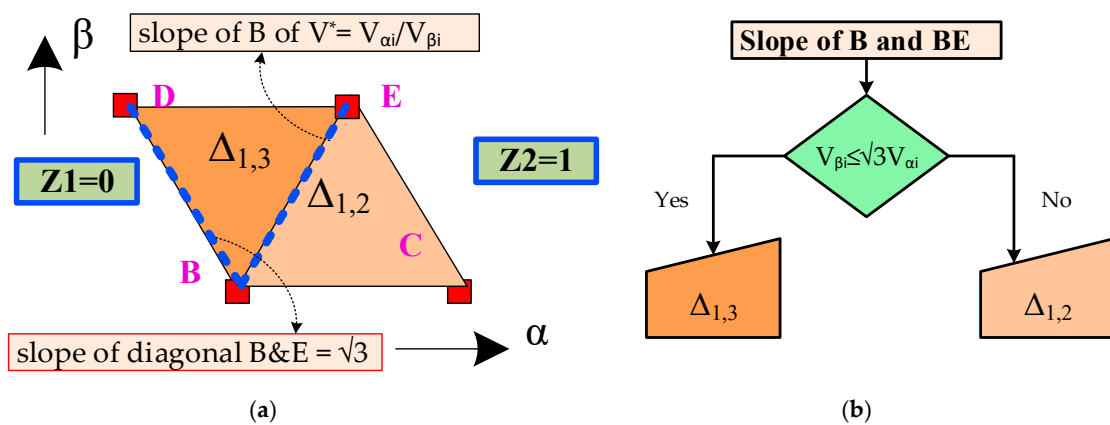


Figure 6. (a). Sector-1 rhombus diagonal slope, (b) flow chart for rhombus sub-triangles selection.

3.3. Sub-Triangle Switching On-time Calculations

The flowchart (See Figure 3) shows the complete interpretation of the sub-triangle lookup table (LUT) identification for Zone-1 and Zone-2. To simplify the switching on-time calculations, all sub-triangles are further considered into two categories based on their base position either bottom or top. The first category is called as group-1 triangles ($\Delta_{1,1}$, $\Delta_{1,2}$ and $\Delta_{1,4}$), where it has a base at the bottom. Similarly, group-1 triangle ($\Delta_{1,3}$) is placed in SVD with the base side at the top. Figure 7 shows the group-1 and group-2 triangle for the calculation of switching on-times. For the group-1 and group-2 triangle valuations, the proposed SVM uses simply the calculation by using Zone-1 and Zone-2 triangle positions.

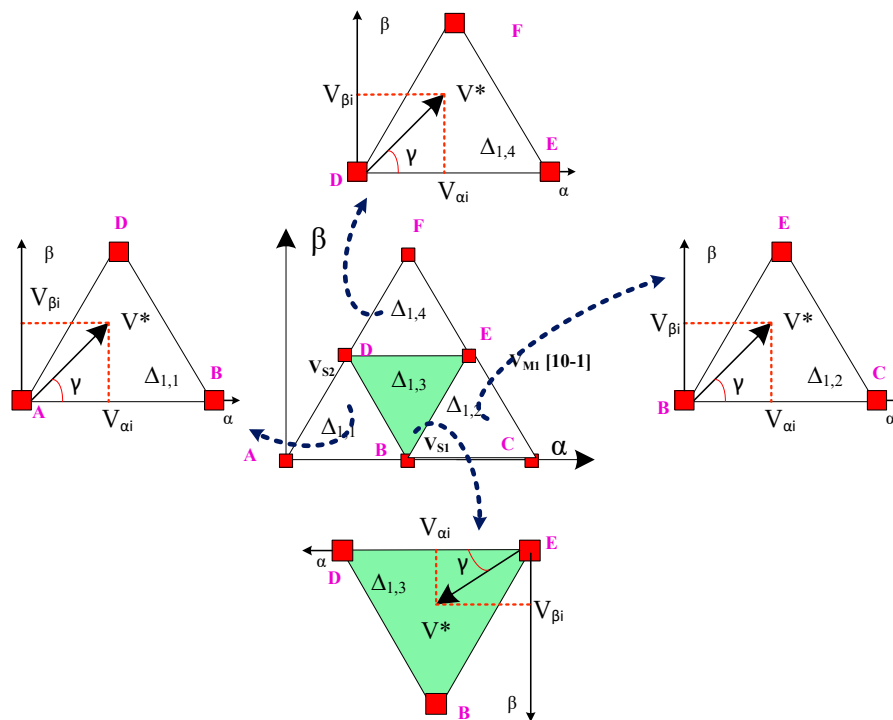


Figure 7. Group-1 triangles ($\Delta_{1,1}$, $\Delta_{1,2}$ and $\Delta_{1,4}$) and Group-2 ($\Delta_{1,3}$) triangle representation for sector-1.

The group-1 triangle is determined by solving the following Equations (9) and (10),

$$\text{int}(\text{zone1})^2 + 2 \text{int}(\text{zone2}); \text{ either } \Delta_{1,1}, \Delta_{1,3} \text{ and } \Delta_{1,4} \quad (9)$$

Else,

$$\text{int}(\text{zone1})^2 + 2 \text{int}(\text{zone2}) + 1; \text{ either } \Delta_{1,2} \quad (10)$$

Thus the coordinates of group-1 triangle and group-2 triangles can be calculated as $V_{\alpha i}^s$, $V_{\beta i}^s$ and $0.5 V_{\alpha i}^s$, $h - V_{\beta i}^s$.

From the individual sub-triangle α , β coordinates, the switching states on-time of each sub-triangle can be calculated similarly to two-level SVM.

$$T_1 = T_s(V_{\alpha o}^s - V_{\beta o}^s / \sqrt{3}) \quad (11)$$

$$T_2 = T_s(V_{\beta o}^s / h) \quad (12)$$

This calculation can be used for n-level MLI by the accumulation of the group sub-triangles.

3.4. Extending to Over Modulation

To move the V^* from LM to OVM region, the V^* is moved to outside the hexagonal trajectory. During this circumstance, the M_a is valued more than 0.9 and the V^* moves outside SVD hexagonal boundary. Thus, the synthetization of V^* in the OVM region is unrealistic (non-linear nature movement). As a result, to achieve the OVM region operation and calculating its switching state on-times, the traditional approach used trigonometric functions to calculate the OVM voltage vector switching state on-times [20,24,30]. These methods consume more mathematical and implementation complexity. In addition, these methods are producing higher low frequency harmonics. The proposed OVM method has a straightforward nature to realize switching on-time from the LM switching time. Hence the non-linearly can be minimized, which helps to avoid the additional lower frequency harmonics. The OVM region is operated in two zones as OVM-1 (V^* is lies from 0.908 to 0.958) and OVM-2 (V^* is lies from 0.958 to one).

In the OVM-1 region, as shown in Figure 8, there would be portions of the OVM line cycle, which are placed partly within the SVD hexagon and partly outside the hexagon. Hence the two relations are derived for calculating the on-time for V^* circular region and hexagonal region. To differentiate these two boundaries, the crossover angle (θ_c) is calculated from the reference vector M_a ,

$$\theta_c = 30^\circ - \cos^{-1}(\Pi/(2\sqrt{3}M_a)). \quad (13)$$

Now the V^* angle θ fulfills the position $\theta_c \leq \theta < \Pi/3 - \theta_c$, the V^* remains in hexagonal trajectory, and another portion follows the circular trajectory ($0 \leq \theta < \theta_c$ to $\Pi/3 - \theta_c \leq \theta < \Pi/3$). Based on the V^* position in SVD, the OVM-1 coordinates (V_α and V_β) of V^* can be calculated from θ and level (n),

$$V_\alpha = (\sqrt{3}(n-1))/(\sqrt{3} + \tan \theta), \quad (14)$$

$$V_\beta = (\sqrt{3}(n-1) \tan \theta)/(\sqrt{3} + \tan \theta). \quad (15)$$

From the V_α and V_β , the $V_{\alpha o}^s$ and $V_{\beta o}^s$ are calculated for deriving modified switching on-time,

$$T_1 = T_s(V_{\alpha o}^s - V_{\beta o}^s/\sqrt{3}); T_0 = 0; T_2 = T_s. \quad (16)$$

To realize the circular trajectory and hexagonal trajectory switching on-times, the gain factor (G_t) can be calculated from the OVM-1 maximum boundary and its actual M_a values. The maximum volt-seconds loss in OVM-1 region is proportional to (0.9535 – 0.907). Hence, the G_t can be obtained from LM M_a as,

$$G_t = (OVM - 1 - 0.907)/(0.9535 - 0.907). \quad (17)$$

Adding and subtracting the G_t with T_0 , T_1 and T_2 , the circular trajectory and hexagonal trajectory switching on-time can be calculated by modifying the V^* .

Now from Equations (11), (12), and (17), the hexagonal trajectory switching on-time is derived as,

$$T_{1 \text{ OVM-1 HT}} = T_s(V_{\alpha o}^s - V_{\beta o}^s/\sqrt{3}) + 0.5G_t^2T_o, \quad (18)$$

$$T_{2 \text{ OVM-1 HT}} = T_s(V_{\beta o}^s/h) + 0.5G_t^2T_o, \quad (19)$$

$$T_{0 \text{ OVM-1 HT}} = T_s - T_{1 \text{ OVM-1 HT}} - T_{2 \text{ OVM-1 HT}}. \quad (20)$$

Similarly, the circular trajectory switching on-time is derived as,

$$T_{1 \text{ OVM-1 CT}} = T_s(V_{\alpha o}^s - V_{\beta o}^s/\sqrt{3}) - 0.5G_t^2T_1, \quad (21)$$

$$T_{2 \text{ OVM-1 CT}} = T_s(V_{\beta o}^s/h) - 0.5G_t^2T_2, \quad (22)$$

$$T_{O\text{ OVM-1 CT}} = T_s - T_{1\text{ OVM-1 HT}} - T_{2\text{ OVM-1 HT}}. \quad (23)$$

When the V^* modulation index M_a is more than 0.9535, then the V^* is entered into OVM-2 region. During this time the V^* is allowed only in the hexagonal trajectory (beyond the OVM-1 HT), and only six LVs are needed to operate. Hence, the holding angle (θ_h) is derived using a similar strategy [9] to keep the V^* at one of the large vectors. The relations $0 \leq \theta < \theta_h$ and $\Pi/3 - \theta_h \leq \theta < \theta_h$ help to find one of the LV in the particular sector with changing V^* position. The on-time equations of OVM-2 are obtained as,

$$0 \leq \theta < \theta_h; T_1 = T_s, T_2 = T_o = 0, \quad (24)$$

$$\Pi/3 - \theta_h \leq \theta < \Pi/3; T_2 = T_s, T_1 = T_o = 0. \quad (25)$$

The proposed LM and OVM do not change V^* position. Hence, it allows simple implementations.

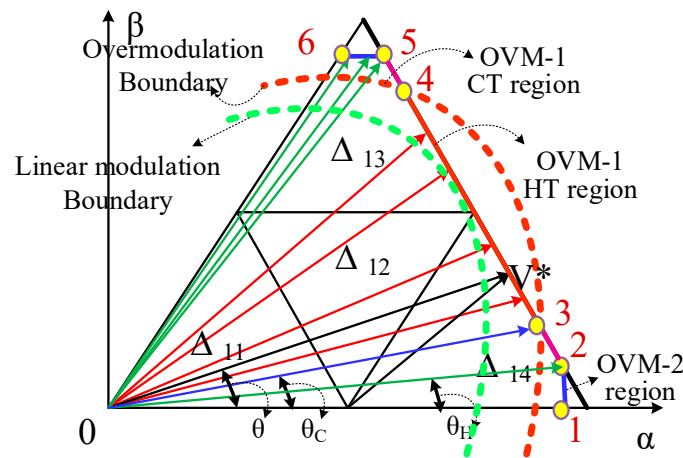


Figure 8. OVM boundary for proposed three-level SVM.

4. MATLAB-Simulink Implementation of Three-level SVM

The proposed MLI SVM design is established using MATLAB 13.b Simulink with five subsystems that are connected through In and Out Xilinx SG that helps to implement the MLI SVM directly from MATLAB-Simulink (.mdl) file to target FPGA. Figure 9 illustrates the detailed MATLAB-Simulink design flow of proposed MLI SVM.

- 1) The first block is the “Clarke’s transformation”, in which the three-phase reference rotating frame are converted into V_α, V_β .
- 2) The 2nd block named ‘Sector and γ identifier’ block holds four sub-systems namely reference vector M_a , θ , sector and γ .
- 3) The next block is calculating the local vector reference frame ($V_{\alpha 0}^s$ and $V_{\beta 0}^s$) and finding the sub-triangle. Then the switching on-times T_1, T_2 , and T_0 are calculated (based on two-level SVM).
- 4) The fourth subsystem is calculating the LM and OVM boundary based on the reference vector M_a . The subsystem receives the sub-triangles, $V_{\alpha 0}^s$ and $V_{\beta 0}^s$ to sample switching pulse period for the T_s . The switching events of all 27 switching states are stored in LUT.
- 5) Finally, based on the sector number, sub-triangle number, and M_a boundary, the switching on-times are calculated and mapped into the corresponding switching states.

The performance of the MLI SVM for $0 < M_a \leq 0.99$ is simulated on a three-level NPC-MLI drive with 460V DC-link, two 470 μF DC-link capacitors, and 10 kHz switching frequency. The 2.45 kW, 1440 rpm, four poles, and 50 Hz induction motor is used as a load. Figure 10 shows the inverter line voltage (V_{uv}) waveform for LM, OVM-1 and OVM-2 operations. Initially, the simulation studies are conducted for $M_a = 0.5$. Here the line voltage (V_{uv}) is measured as a 2-level output, because only

the SVs and ZVs have participated in the switching sequence. Hence, the V_{uv} resulted in 2-level output was 147.8 V with THD value of 13.06 %. Next, the same simulation study is extended for the higher modulation ranges (more than 0.5) and resulting in increased voltage magnitude. When the inverter is operated at maximum LM range of 0.907, the V_{uv} resulted is 268.4 V, as shown in Figure 10. As expected, the fundamental voltage is increasing linearly by increasing M_a . Here the line voltage at $M_a = 0.950$ and $M_a = 0.990$ is observed as 282 V and 295 V, respectively.

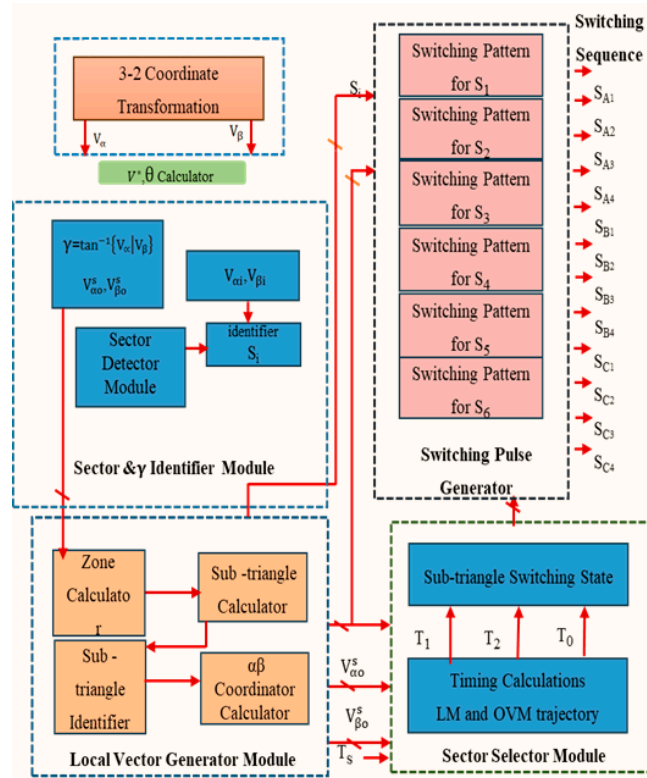


Figure 9. MLI SVM MATLAB-Simulink implementation flow chart.

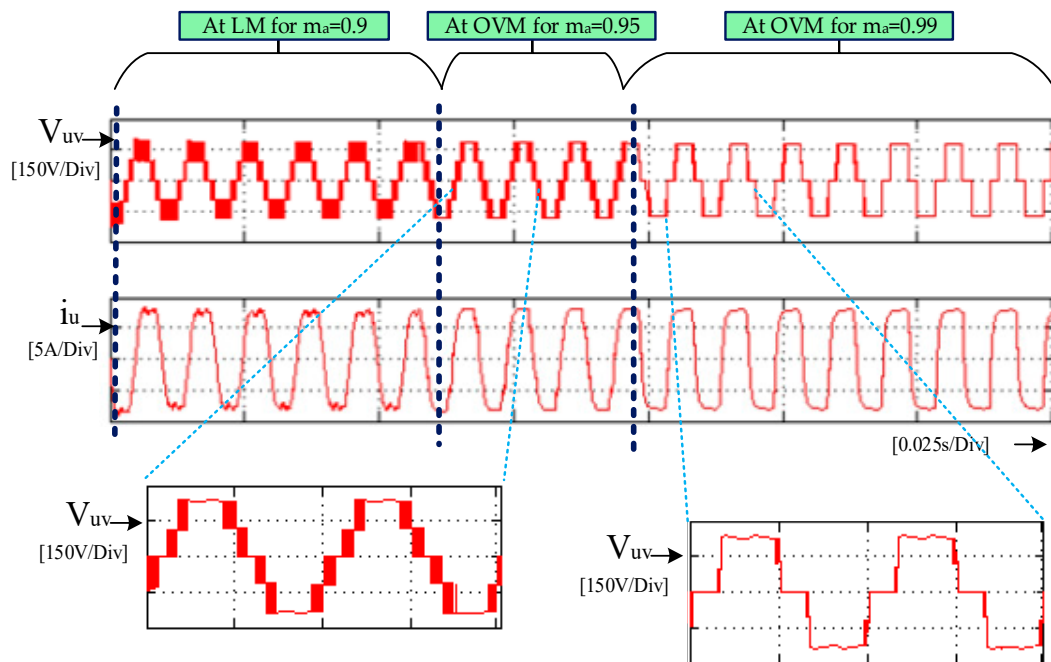


Figure 10. Simulation result for modulation range ($0.9 < M_a \leq 0.99$).

5. FPGA Collaborated Experimentation Setup of Three-Level MLI

The experimental setup diagram and FPGA are collaborated Three-phase three-level NPC MLI is shown in Figure 11. The NPC-MLI is designed with three integrated surface-mounted SK100MLIO66T-SEMIKRON four IGBT modules.

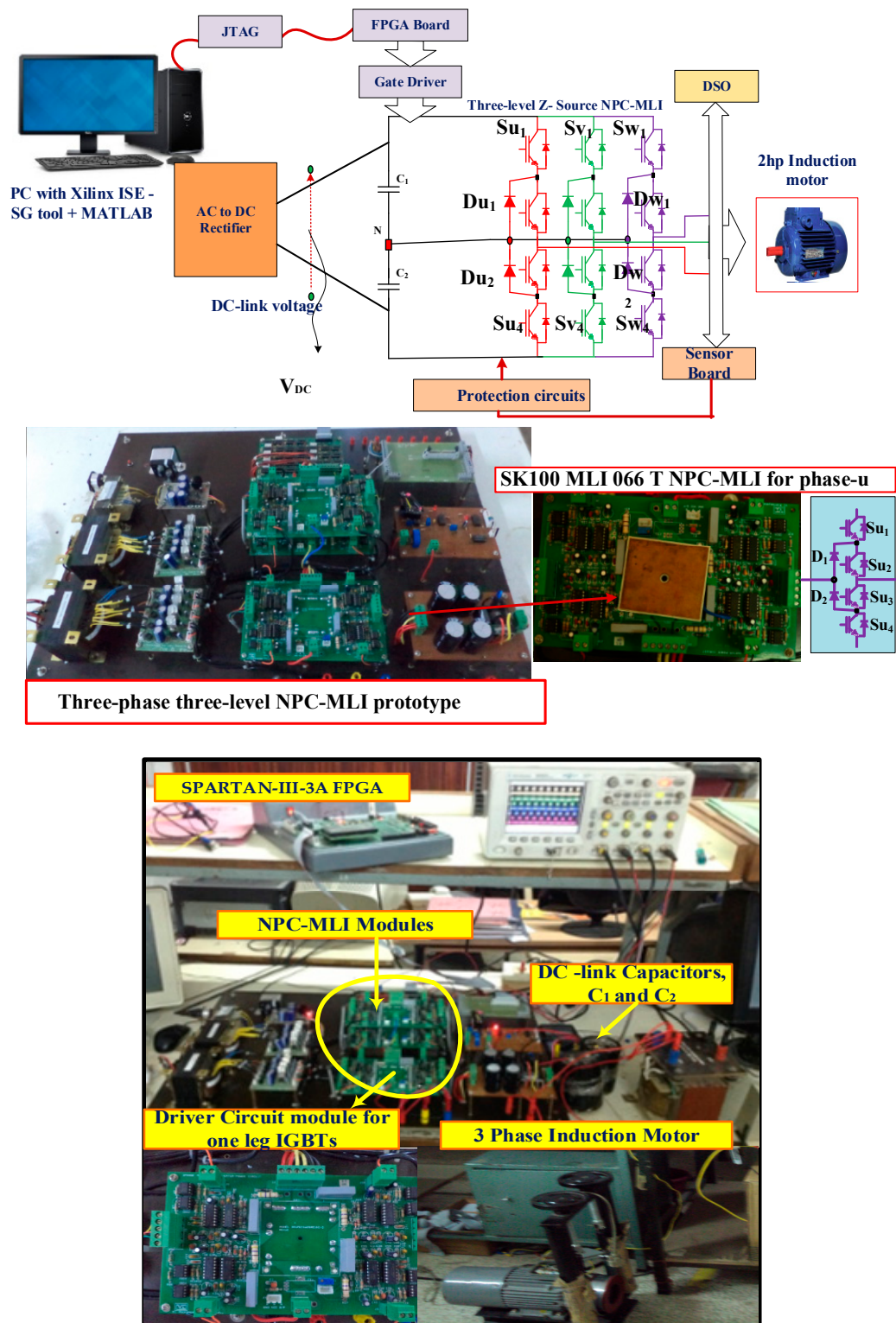


Figure 11. Three-level MLI experimentation with SPARTAN-III-3A XC3SD1800A-FG676 DSP-FPGA.

Two 100 μF , 1000 V rating DC-link capacitors are used for providing DC-link voltage of the MLI. The switching module used HCPL4506 opto-isolator to provide the isolation between the FPGA controller, and IGBT. The Xilinx family SPARTAN-III-3A XC3SD1800A-FG676 DSP-FPGA controller is used to implement and generate the proposed SVM. The 2.45 kW, 1440 r/min, 50 Hz, 4-pole three-phase squirrel-cage induction motor (SCIM) drive is used as a load. The YOKOGAWA spectrum analyzer is used for capturing the experimental results.

6. MATLAB-Simulink built FPGA Habitat for Hardware Implementation

The MATLAB-Simulink support Xilinx ISE project navigator system generator (SG) tool is used for the proposed SVM implementations as it allows the minimization of the time spent for design and cost of implementation.

The architecture of the proposed SVM FPGA implementation is shown in Figure 12. The FPGA core contains the two main modules: (1) The processing unit; and (2) switching and its mapping unit, as shown in Figure 13. These modules can perform in parallel that helps to minimize the processing time. The processing unit comprises functional blocks to calculate the V^* , sector, sub-triangle, $\alpha\beta$ coordinates for LM and OVM trajectory, and logical routes. The mapping unit consists of switching vectors for the corresponding sub-triangles. The switching vector-mapping unit uses memory (LUT). It maps the pre-stored switching sequence for the MLI based on sector, sub-triangle.

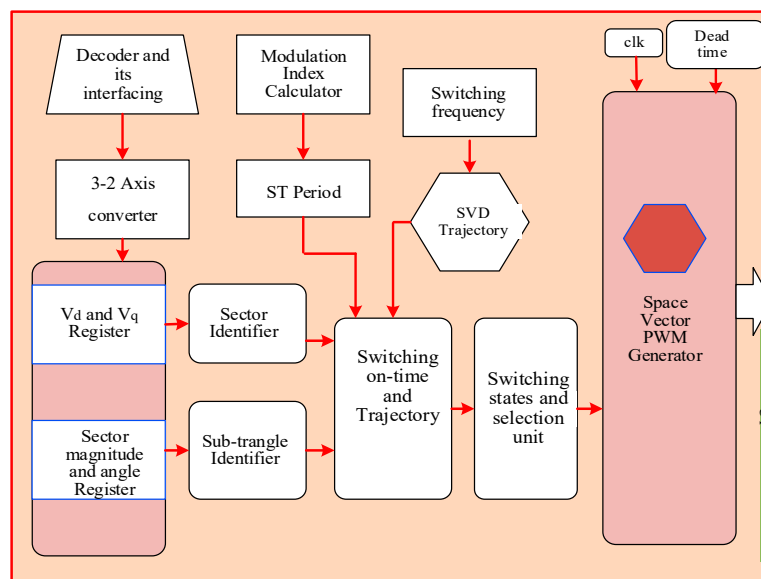


Figure 12. Proposed MLI SVM FPGA core structure.

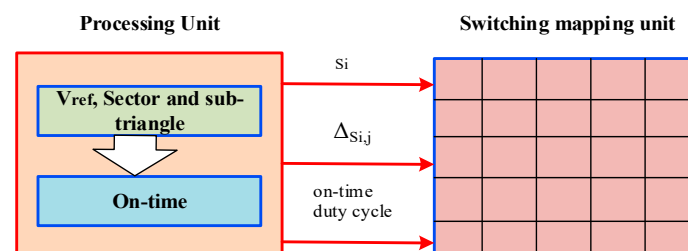


Figure 13. Processing unit and mapping unit sharing.

The core also considers some key design measures for improving computation accuracy and simplifying hardware design and the fixed-point arithmetic unit is adopted for implementing the calculations. The IP core is designed to operate at 20MHz clock frequency, and high switching

frequency, as well as the t_d , is adjustable. The architecture of the proposed SVM sub-blocks is described, as follows:

1. 3/2 axis converter block: It performs the abc to d-q conversion, which generates the V^* and angle (θ).
2. M_a block: Depending upon the V^* requirement, the M_a value of the inverter can be given through the M_a block.
3. Switching period block: It holds the sampling frequency for the inverter switches.
4. Sector identification block: This block finds the V^* location based on the angle (θ) and V^* magnitude.
5. Triangle identifier block: The block computes V^* sub-triangle location.
6. Trajectory identifier block: This block measures the trajectory identifier (LM, OVM boundary) and V^* location based on the M_a values. It also calculates θ_C and θ_H angles for OVM operation.
7. On-time calculation block: This block calculates the respective switching state on-times based on two-level SVM calculations. This unit uses the LUTs to store the switching states and the switching sequences. Lastly, SVM generator unit generates the pulses to the 3-level NPC-MLI after inserting the dead time (t_d).
8. Switching state unit: It holds the 27-switching event.
9. Dead time register block: Holds the timer to add or reduce the t_d .
10. SVM Generating Unit: This block produces the pulses to the NPC-MLI after inserting the t_d .

To simplify the interface with the processor, commands to these registers are routed through a decoder and interface circuit. The clock is acting as a base time for PWM generator and is operated at 100MHz. The overflow flag from PWM generator unit indicates the value of PWM counter when it reaches the maximum count, which can be used to trigger events for the inverter.

6.1. Implementation of the Proposed MLI SVM Scheme in FPGA

The XSG FPGA environment implementation is divided into five stages as follows: MATLAB code generation through XSG, VHDL code generation and its simulation, register transfer level (RTL) file and bit file generation, synthesis and download into target FPGA. Once the RTL file is generated, the proposed SMV architecture RTL view (shown in Figure 14) and off-line simulation is done to view the generated inverter pulses using ModelSim 5.8e. Figure 15 shows the ModelSim simulation results for the proposed MLI SVM. It ensures the desired pulse pattern, t_d values. After successful synthesis, the device utilization and power utilization report is generated. It provides the number of logical blocks, LUTs and FFs to be used in architecture. The proposed MLI SVM uses only 3.7% LUT memory space in the FPGA, since it uses simple 2-level SVM, and hence, does not require any additional calculations for calculating the switching on-time. It also minimizes the processing time for LM and OVM operations. Figure 16a shows the internal structure based on the described SVM implementation design. After RTL synthesis, the net list is saved as an NGC file. Afterwards, the JTAG serial mode ("IEEE Standard 1149.1") configuration interface card is used to download the code to the Target FPGA SPARTAN-III-3A XC3SD1800A-FG676. The JTAG configuration is through the independent boundary scan selection. Then the regenerated bit file is generated. Finally, the developed RTL is converted to bit stream format, and then the UCF is written for pin assignment for the mapping process. Mapping is done to fit the design into the available resource of the target FPGA processor. Finally, placing the code in target FPGA is done.

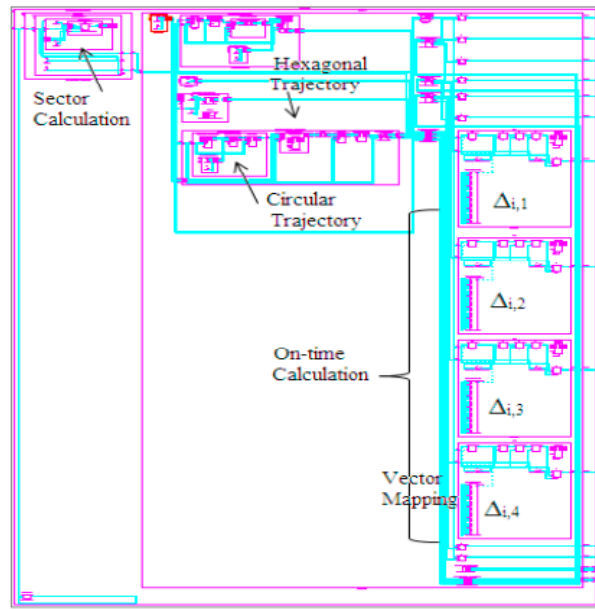


Figure 14. Register transfer level (RTL) view proposed MLI SVM core.



Figure 15. ModelSim simulation results; 12-pulses (S_{1u} – S_{4w}) of proposed MLI SVM for $f_s = 10$ kHz, dead time = 6 μ s.

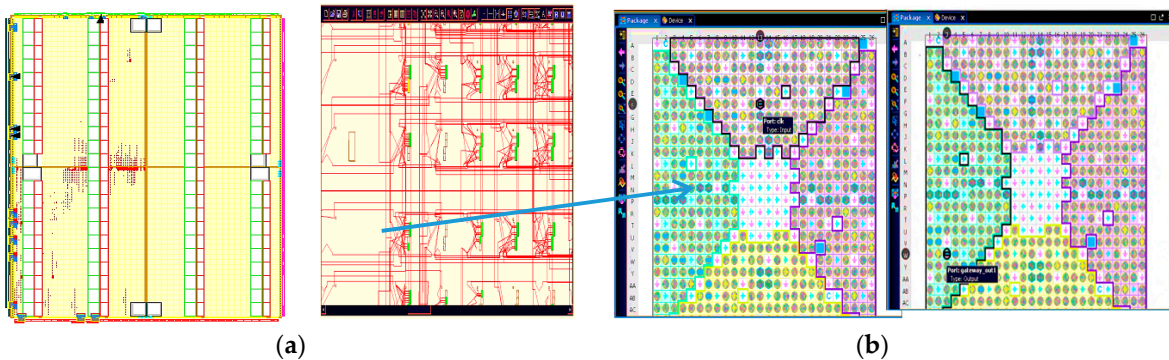


Figure 16. (a) Device area utilization, (b) input and output port view for the implemented SVM.

6.2. MLI SVM FPGA Implementation Results

There are three types of floor views that are generated for the SVM IC, which are overall floor view of device utilization, input port assign view, and output port assign view. From Figure 16a, it is observed that the proposed code occupies very less resource/area. Figure 16b shows the input and output port of the proposed implementation. The proposed PWM design I/O's are mapped properly using UCF based on reduction of the power losses. The implementation consumes only 0.13 W power utilization for one cyclic operation of pulse generation.

Due to the simplification of sub-triangle calculations and OVM-1 switching mapping, the overall device utilization of the proposed SVM implementation becomes 5.88%, which is less than the earlier

implementations [14,23,40,45]. The simplified calculation to find the rhombus sub-triangles selection and OVM-1 on-time calculations are the primary reasons for the memory reduction (around 0.17%), while considering the implementation reported in [23]. The additional reductions are achieved by way of reducing the LUT usage for operation by repeating switching states.

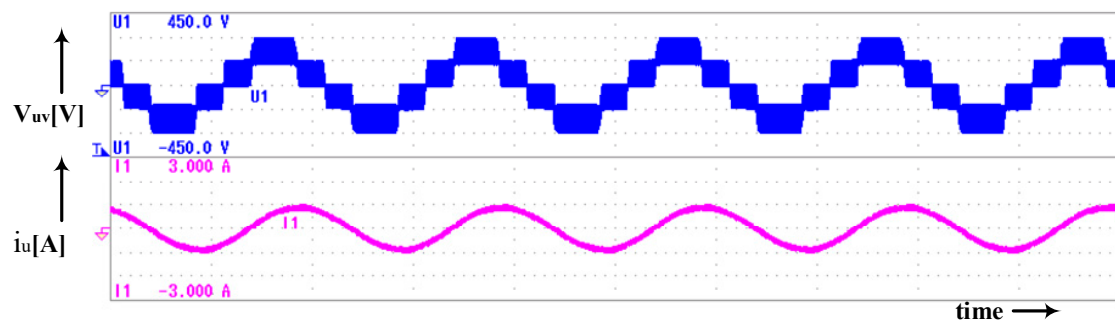
The processing time of the proposed implementation for LM OVM-1, and OVM-2 are calculated using [37], and the values are 13.017 μ s, 14.561 μ s, and 15.532 μ s, respectively. From the results, it can be understood that the proposed FPGA implementations are taking the same time for all LM values as 13.017 μ s, since sub-system calculation is same for all the range of LM from 0.5 to 0.907. However, during over modulation operations, the processing time for the proposed implementation is increased. The increase in time is because of G_t calculation for the new on-times. Nevertheless, when compared to the early implementations, the time taken for OVM is less for the proposed method [23], and it is expected while implementing with other family FPGAs. Similarly, considering the device utilization (memory occupied) on FPGA for the proposed implementations, it is considerably lesser. From the above analysis and results, it is clear that the proposed MLI SVM algorithm and its Spartan-3 FPGA implementation improved in terms of their owning mathematical complexity and implementation. Hence, due to this reduced mathematical burden, less device utilization and processing time, the proposed implementations fit to be considered as an IP core that can be incorporated into a System On-Chip with other IP cores and it can greatly reduce the area of a PCB and improve the immunity to interferences for the power converters design.

7. Experimental Results and Analysis

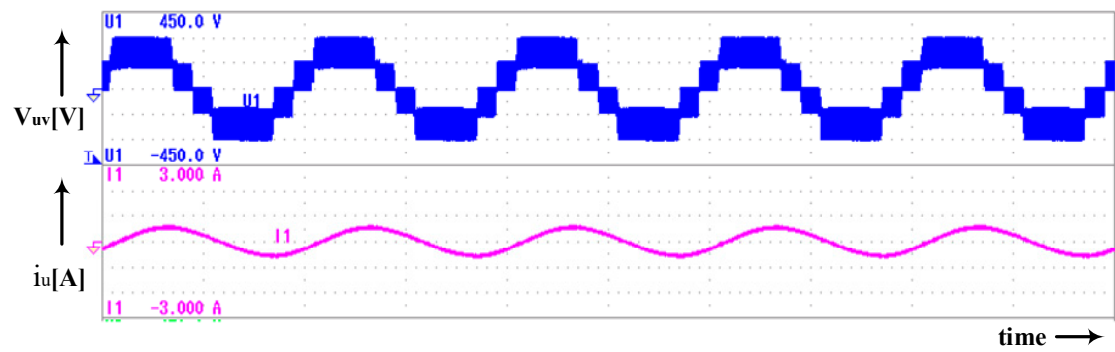
In order to validate the proposed MLI SVM FPGA implementation, the experimentation study is conducted for 2.3 kW three-phase induction motor supplied from three-phase three-level NPC-MLI. The DC-link voltage of the NPC-MLI is maintained at 560 V through an uncontrolled rectifier. The two 100 μ F DC-link capacitors C_1 and C_2 are connected with DC-link to clamp the voltage. The switching frequency of 10 kHz and dead time of 6 μ sec is used between two complementary switches. The experiment study is performed with modulation index value from 0.7 to maximum over modulation range ($M_a = 0.99$). During the study, the speed of the motor is recorded using digital tachogenerator.

Figure 17a–d depicts the experimental results of MLI line-voltage (V_{uv}) and corresponding current (I_u) for $M_a = 0.7$, $M_a = 0.9$, $M_a = 0.95$, and $M_a = 0.99$, respectively. In the LM region, the inverter output voltage is obtained as 205.2 V and 262.4 V for $M_a = 0.7$ and $M_a = 0.9$, respectively. However, while increasing the M_a from LM to OVM, the fundamental voltage is increased linearly. The V_{ab} for $M_a = 0.7$ and $M_a = 0.9$ is obtained as 280.3 V and 292.5 V, respectively. From the results, it can be seen that the inverter voltage and current waveforms are changing based on the modulation index value.

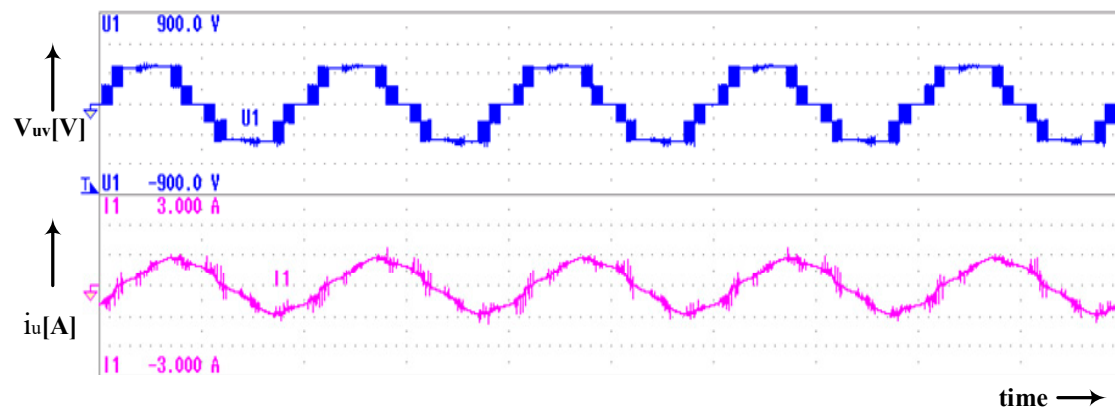
However, the voltage and current waveforms are smooth in all the range of modulation indices. This demonstrates that the proposed SVM is working with full control degree of freedom in the linear and over modulation region. Figure 18a–d shows the voltage and current harmonics spectrum. The voltage and its corresponding current harmonics in the LM are lesser when compared with those in the OVM regions. The line voltage percentage THD is observed as 10.2%, 12.9%, and 13.5% for $M_a = 0.9$, $M_a = 0.95$ and $M_a = 0.99$, respectively. This increase is due to the non-linearity in the switching on-times in the OVM region operation. Similarly, the current percentage THD in OVM is higher than that in LM. When compared with the other multicarrier and selective harmonics elimination PWM methods, the proposed SVM has lower current and voltage THD in both LM and OVM. In addition, while changing the inverter operation from one region to another region, the voltage and current waveforms are smooth, and there are no abrupt changes.



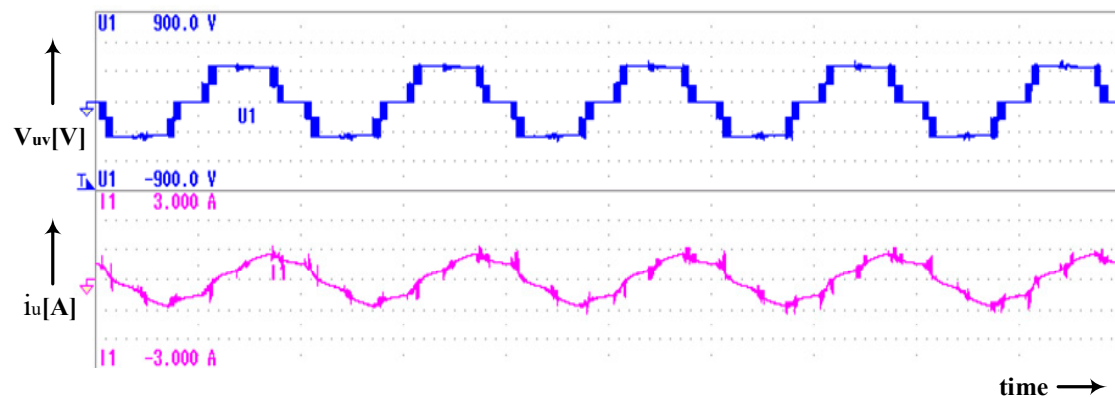
(a)



(b)



(c)



(d)

Figure 17. Line voltage (V_{uv}) and Phase current (I_u) waveform; (a) V_{uv} for $M_a = 0.7$, (b) V_{uv} for $M_a = 0.9$, (c) V_{uv} for $M_a = 0.95$, (d) V_{uv} for $M_a = 0.99$.

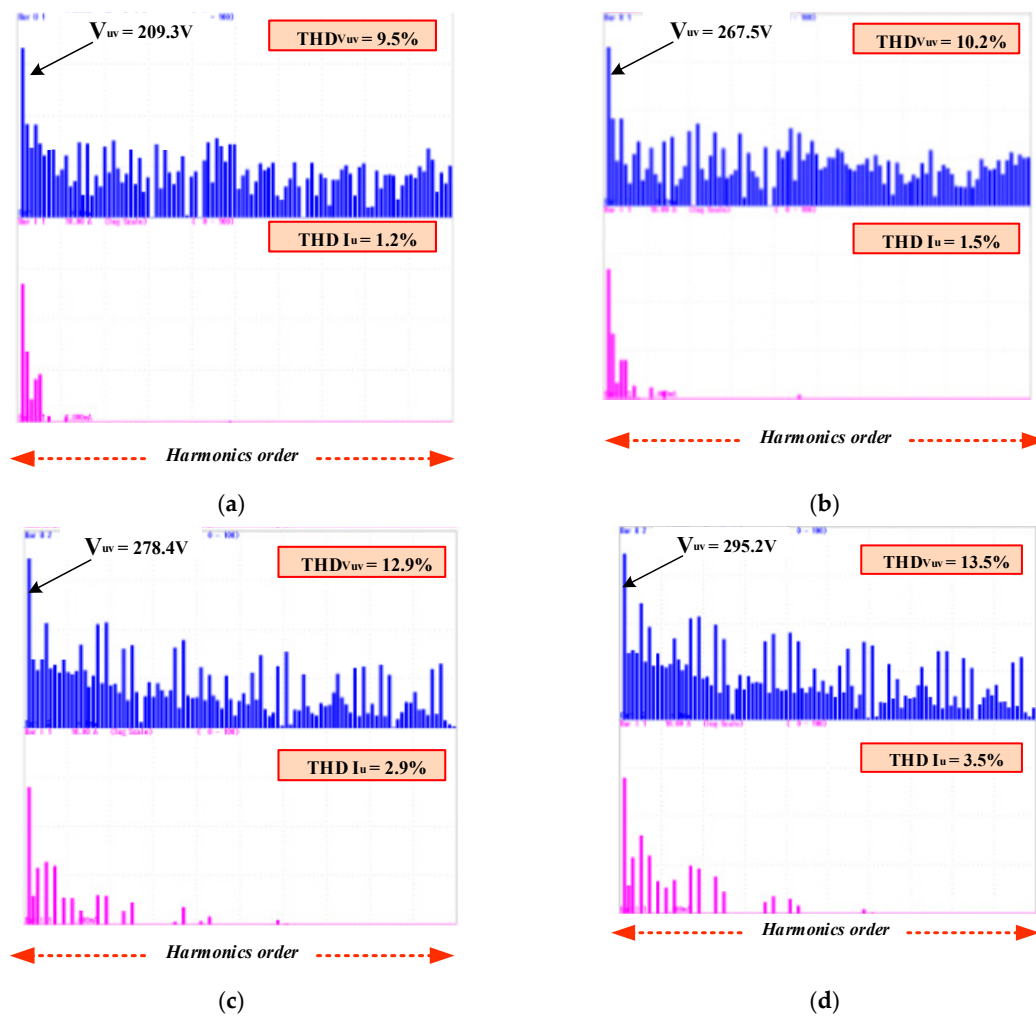


Figure 18. Line voltage harmonics spectrum; (a) at $M_a = 0.7$, (b) at $M_a = 0.9$, (c) at $M_a = 0.958$, (d) at $M_a = 0.997$.

The induction motor speed variations for the modulation index range from $M_a = 0.7$ to $M_a = 0.99$ are measured and plotted in Figure 19. From the results, it can be seen that the motor speed changes in linear with the SVM modulation index. This illustrates that the proposed SVM can be directly employed to open-loop drives. In closed-loop operation, depending on the control requirement, the proposed SVM voltage reference magnitude and frequency can be changed easily without any additional mathematical calculations.

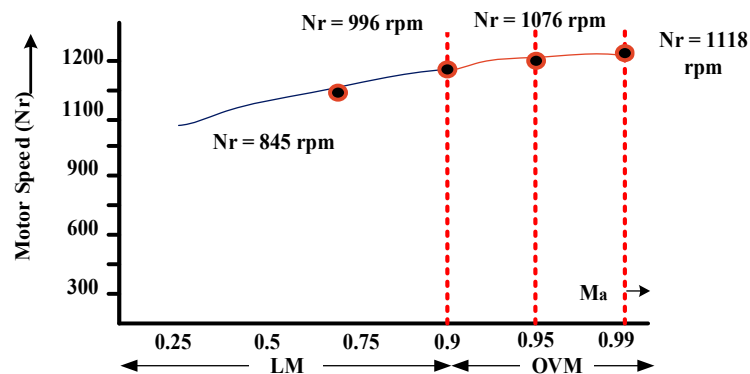


Figure 19. Motor speed response while changing modulation index.

8. Conclusions

In this paper, the detailed theoretical analytical study on MLI SVM and its digital implementation practices are explained. In addition to the previous method of SVM, the paper has also proposed a simplified mathematical approach to find out the MLI SVD sub-triangles, switching on-time calculation in both linear and over modulation. The proposed three-level MLI-SVM is exhibited based on two-level SVM without changing the reference vector position, unlike the traditional approaches. Hence, it can be easily prolonged with additional LUTs for any n-level inverter without any significant increase in computations. The proposed MLI SVM is comprehensively analyzed and validated for implementation in Xilinx family SPARTAN-III-3A XC3SD1800A-FG676 FPGA. The mathematical procedure involved in the proposed MLI SVM is reduced compared to the early attempts; hence, the device utilization and processing time are considerably reduced. The MATLAB–Simulink SG based simulation and SPARTAN-III-3A XC3SD1800A-FG676 FPGA implementation are performed to validate the proposed SVM with 2 kW three-phase three-level NPC MLI fed induction motor drive system. The presented results are confirming the performance of the MLI SVM at different modulation depths of the NPC MLI. The proposed implementation fits to be considered as an IP core that can be incorporated into a System On-Chip with other IP cores.

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Nomenclature

| | |
|---------------------------------|---|
| V^* | Reference vector |
| V_α, V_β | Voltage vectors stationary reference frame |
| δ_{VS2} | Duty cycle of SV |
| δ_{VM2} | Duty cycle of MV |
| δ_{VL2} | Duty cycle of LV |
| Δ_{ij} | Sub-triangle within the sectors |
| θ | Angle of the reference vector |
| γ | Sector angle |
| h | Vertices height |
| $V_{\alpha o}^s, V_{\beta o}^s$ | Individual Sub-triangle α, β coordinates |
| θ_C | Crossover angle |
| θ_h | Holding angle |
| PWM | Pulse Width Modulation |
| MLI | Multilevel Inverter |
| SVM | Space Vector Modulation |
| SVD | Space Vector Diagram |
| LM | Linear Modulation |
| OVM | Over Modulation |
| NPC | Neutral-Point Clamped |
| ZV | Zero Vector |
| SV | Small Vector |
| MV | Medium Vector |
| LV | Large Vector |
| IP | Intellectual Property |
| HT | Hexagonal Trajectory |
| CT | Circular Trajectory |
| THD | Total Harmonic Distortion |
| IGBT | Insulated-Gate Bipolar Transistor |
| SCIM | Squirrel-Cage Induction Motor |

| | |
|-----|-------------------------|
| SG | System Generator |
| RTL | Register transfer level |
| LUT | Lookup Table |

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